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Reliability Analysis of Minimal Hammock-based Logical Gate Networks

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Abstract

For a given system, reliability is defined as the system's ability to remain in its operational state after failure in some of its components. In other words, reliability is closely related to resilience, robustness and fault-tolerance. Moore and Shannon introduced a probabilistic model in which network nodes are assumed to be completely reliable and communication links or edges can fail with a given probability such as *p*. The main problem is determining the probability that the network will remain connected under these conditions; it means establishing a route between the source and destination terminals. If all links are operational with the same probability of *p*, the reliability of the entire network is described as a function of *p*, which in turn leads to the reliability polynomial of network. Moore and Shannon proposed their reliability analysis on specific networks known as hammock networks. Such networks can be well adapted to array-based circuits such as FinFET, VSFET, MOSFET, NEMS and CNFETs. In this article, focusing on hammock networks, we use their combination to design and implement MOS-based transistors, i.e., nMOS and pMOS, and implement basic logical gates based on such networks. To determine the reliability polynomial coefficients, various methods have been presented that most of them have computational complexity due to the recursive property. Practically, for circuits with large order and size, the exact calculation of reliability polynomial coefficients is in the NP-hard complexity class. In this study, while reviewing the existing problems, efficient methods have been used to determine the polynomial coefficients of reliability. In order to make the comparisons and evaluations fair and accurate, with the help of simulation results, performance and reliability measures were extracted for all circuits and the reliability of the investigated networks has been compared and analyzed.

Keywords: Network reliability, Hammock networks, Reliability polynomial, Logical gates

1. Introduction

In the current era, when the speed and volume of communication and information have grown incredibly, communication systems and infrastructures are mainly struggling with many problems that classical methods are unable to answer. These reasons have caused great attention and movement towards interdisciplinary trends such as data analysis and networks based on graph structures. To build any successful communication network, different aspects should be taken into consideration. Therefore, important factors such as cost, security, safety, integrity, scalability, fault-tolerance and reliability can be mentioned and the latter one is especially important for any communication network. In this way, the issue of robustness and reliability of networks has been given considerable importance in the conducted studies recently [1].

A system is robust if it has the ability to maintain its main and basic functions even in the presence of external or internal errors. In the network area, the robustness of the system refers to its ability to perform the main assigned tasks, that even after removing a part of its nodes or edges, it remains connected as much as possible from a global perspective[2]. Also, resilience is defined as the ability of any entity in the network to tolerate and soften (resistance and automatic recovery) against severe changes in that network and its applications [3, 4].

So far, various criteria have been suggested to evaluate the resilience of networks, and an important part of these measures has been devoted to graph theory [5]. In this manuscript, we will use the reliability polynomial criterion to analyze the reliability of circuits and networks based on logical gates, which are the main building blocks in arithmetic circuits. The effort is to provide a set of conceptual and practical tools to analyze and evaluate the reliability of circuits from their compliance with research and practical fields in arithmetic circuits.

Moore and Shannon [6] first proposed the concept of reliability polynomial, it was used to evaluate the reliability in special networks that Moore and Shannon called Hammock networks. They introduced a probabilistic model in which the nodes of the network were assumed completely reliable, but the edges could fail with a given probability (*p*). They introduced the minimal Hammock networks and their main goal was to find improvements in the reliability provided by replacing a single unreliable electromechanical relay (switching element) with an extended network of similar relays. The networks evaluated by

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them had two distinct contacts, which they called input S and terminal T. Hammock networks can be well placed in arithmetic circuits and array-based designs such as vertical FET (VFET), vertical slit FET (VeSFET), as well as FinFETs and NEMS[1], as well as arrays of CMOS components.

Today, when the use of networks is institutionalized in societies, the fundamental idea of Moore and Shannon can be applied to a wide range of networks. Most of the researches have been gathered around this topic and many types of the initial problem have been investigated and analyzed. In general, two main research areas have been discussed in the reliability of networks: analysis and design. The analysis problem deals with explaining the reliability of the network under test; while the purpose of design is to build networks that have high reliability [7]. It is obvious that most of the research work done in this article is focused on the first case.

Dissimilar to the other robustness measures that assign a numerical value (usually normalized) to the resilience of a graph, the advantage of reliability polynomial is that it assigns a function in terms of p, $h(p)$, to each graph. With the curve of this function and its integral within interval [0,1], it is possible to find out about the reliability of graphs and networks and compare them with each other. However, one of the most important and fundamental challenges is that in circuits and networks with a large number of components, it is difficult and even impossible to apply reliability polynomials directly; because determining its coefficients is not an easy task. It should be acknowledged that accurate calculation of reliability polynomial coefficients is easy for graphs with low order; however, its exact solution for networks with high order relies among NP-hard problems. Our main contribution in this research is the use of the efficient methods to determine the reliability polynomial coefficients with low complexity in minimal Hammock networks and then using these networks in the construction of transistors and basic logical gates for construction and implementation of compressors. Accordingly, it is possible to estimate the coefficients of reliability polynomial corresponding to these circuits with appropriate accuracy and low complexity using different numerical techniques and random algorithms. Recently, in another research work [8], we investigated the reliability of various types of arithmetic circuits. In that article, the reliability of various types of compressors and adders has been investigated and we have shown that the reliability of arithmetic circuits can also be calculated using the presented methods.

In the present study, we will first introduce and study small and minimal Hammock networks, and then evaluate the reliability polynomials of such networks and their properties from the theoretical, algorithmic, and design aspects from state of the art. We will first design and implement all basic logical gates according to minimal Hammock networks and then evaluate their reliability. The effort is to make the proposed analyzes as accurate as possible with the help of simulation results. The reliability of logic gates and circuits is calculated and expressed in terms of reliability polynomials, which is a function of the probability of failure in the switching activity of nMOS and pMOS transistors.

This article is organized in seven sections. In Section 2, related work has been explained. The reliability polynomial and model assumptions and its calculation methods are presented in Section 3. Section 4 is dedicated to introducing Hammock networks and their reliability evaluation. In this section, these networks are introduced in details and their polynomial coefficients are carefully determined. Moreover, the most important performance metrics for evaluating the reliability of Hammock networks and the logic circuits based are introduced. Section 5 is dedicated to the design and implementation of transistors and logical gates based on minimal Hammock networks. In Section 6, numerical results obtained from simulation experiments have been analyzed in order to evaluate the reliability of logical gates. Finally, in section 7, conclusions are drawn from this research while the solutions and suggestions are presented as future work to continue the current line of the present research.

2. Related Work

Moore and Shannon [6] first proposed reliability polynomial. The aim of these two researchers was to study in order to create improvements in reliability resulting from replacing an electromechanical relay with two contents (switching device) through a network consisting of n similar relays by creating a connection between input and output terminals. If the coil was not energized, there would be a path with a probability greater than the assumed value of c; on the contrary, if the coil was energized, with a probability lower than the assumed value of a (where $a<c$), a path would be established between the input and the output. They introduced a probabilistic model in which network nodes were assumed perfectly reliable, but communication links could fail with an assumed probability of p.

Cowell et al. [9] have carefully examined the reliability of small Hammock networks using this concept. They showed that array-based designs such as vertical FET (VFET), vertical slit FET (VeSFET), FinFETs and NEMS, as well as arrays of CMOS devices could be well suited to small Hammock networks. N.C. Rohatinovici et al. [10] have shown that that communication in an axon can be modeled with an array of logic gates that each logic gate imitates an ion channel controlled by the gate voltage. These authors estimated the probability of correct communication in such a model by reliability polynomial analysis for logic gate circuits as PGM[2] and showed that one of the applications of the reliability polynomial function can be the reliability estimation of molecular networks for the processing of biological systems information.

Robledo et al. [11] have presented a technique based on interpolation in order to estimate the coefficients of reliability polynomial. They used Newton's method of interpolation and then corrected its coefficients using Hilbert space $L^2[0,1]$. To ensure the correctness of their method, they used the equality of the number of spanning trees with polynomial coefficients

[1] Nano-Electromechanical Systems
[2] Probabilistic Gate Matrix

corresponding to the smallest polynomial power. It has shown that their computational complexity can be done in polynomial time in the best case and the confidence polynomial has a zero root of n-1 iteration order (n is the order of the graph). In addition, Burgos and Amoza [12] have presented and proved a general theory for reliability polynomials.

Using reliability polynomials, Khorramzadeh et al. [13] have analyzed and investigated the effect of network structural motifs on diffusive dynamics such as the spread of infectious diseases. Further, Eubank et al. [14] have used the reliability polynomials to characterize and design networks and have defined a new criterion according to the centrality of nodes and edges called criticality and shown its relationship with network betweenness. They have pointed out that the application of reliability polynomial of a network can be used to target interferences in order to control the spread and epidemics.

Brown et al. [15] have introduced and investigated a measure called the average graph reliability, that is, ATR[3] integral on the interval [0,1]. Their proposed criterion is actually an option for uniformly reliable networks. In fact, since the exact calculation of reliability polynomial coefficients is an NP-hard problem, the authors have presented strategies to bound the average reliability of the network, which do not necessarily require the calculation of reliability polynomials.

Brown and Dilcher [16] as well as Brown and Colbourn [17] have provided reports on the location of the roots of reliability polynomials. Brown and Colbourn [17] presented that all the real roots of the reliability polynomial are located in the complex plane and in a unit disk centered on 1 ($|z\text{-}1|=1$ or exactly in the interval $0\cup(1,2]$). They also conjectured that all complex roots are located in z:$|z\text{-}1|\leq 1$, which Rowell and Sokal [18] rejected this conjecture.

Furthermore, in order to measure the network reliability, Brown in collaboration with Koc and Kooij [19] has determined the inflection points of the network with the help of reliability polynomials. They reported that there is at most one inflection point in the interval (0, 1) and that there are families of simple graphs that may have more than one inflection point. In [20], the same authors have examined families of graphs whose reliability function may cross with the x-axis more than twice.

Page and Perry [21] have presented a method for ranking the important and critical edges in networks with the help of network reliability polynomials. In addition, Chen et al. [22] wrote a short note on [21] and pointed out the redundancy problem in the definition of edge ranking based on the number of spanning trees.

Beichl and Cloteaux [23] presented a randomized approximation algorithm for calculating the coefficients of reliability polynomial and showed that compared to Colbourn's approximation method [24], their proposed method can empirically have a faster convergence rate. In addition, Beichl, in cooperation with Harris and Sullivan [25], has proposed a bottom-up algorithm based on SIS[4] for estimation of reliability polynomial coefficients by selecting spanning tree and adding edges. Their algorithmic complexity is about $O(E^2)$ and a sampling technique is used to reduce the variance. In another study, Harris, Sullivan and Beichl [26] presented a method to accelerate and improve the proposed method based on SIS, which is a general technique for estimating a specific distribution whose samples are provided by a distribution function other than the desired distribution. For a graph with m edges and n nodes, its complexity from the execution order is reported $O(m \log n\ \alpha(\mathrm{m,n}))$.

Safaei et al. [27], while investigating the major issues of the previous methods, have provided four methods for determining the coefficients of reliability polynomial. In the first method, polynomial reliability coefficients are estimated using an iterative method. This method, on average, has an accuracy equivalent to the common methods in the previous studies. In addition, they have proposed an intelligent method to integrate the values of the reliability polynomial coefficients while the values of polynomial coefficients for smaller indices, larger indices, and intermediate indices have been estimated and calculated with the help of this method. In the third proposed idea, they have used Benford's law in order to integrate numerical values. In the fourth approach, they have estimated the values of reliability polynomial coefficients with appropriate accuracy and efficiency using the Legendre interpolation method.

From what we briefly presented on the related work above, it is understood that after half a century of the seminal work of Moore and Shannon [6], extensive studies in this field have been reported and compiled. Many related issues are related to the main issue are placed for review, generalization, analysis. Our effort in this section was to review important concepts, researches, and results related to the main article, as well as some of the most important developments in the field. For this reason, we have mentioned only some of the most important research directions. It should be acknowledged that although several methods have been proposed in the related work to calculate the reliability polynomial coefficients, we could not ignore the fact that these calculations will practically become an intractable subject with the increase in the size and order of the graph.

3. Preliminaries and Model Assumptions

Networks can be modeled with graphs. In terminology, the ordered pair graph $G(V, E)$ is considered, where V refers to the set of nodes and $E \subseteq \binom{V}{2}$ to the set of links. If $E \subseteq V \times V$, then we have a directed graph in which the edges are called arc. Due to the nature of input and output and propagation of signals, most arithmetic circuits can be viewed as a directed graph. However, in a simple graph, multiple edges are not allowed; if it is allowed, we will face a multigraph. Additionally, if loops are also allowed, we will have a pseudograph. Edges can also have weight, in which case the graph is called a weighted graph. Weight can refer to the length, cost, reliability, price, or anything related to edge graph. In this study, it is assumed that the graphs extracted from arithmetic circuits are directed but simple and unweighted, as well as self-loops.

[3] All Terminal Reliability
[4] Sequential Importance Sampling

Usually, there are three solutions to measure the reliability network. Two-terminal reliability (2TR), all-terminal reliability (ATR) and *k*-terminal reliability (KTR), which are introduced in [6] by Moore and Shannon. In 2TR mode, it is assumed that there are two distinct nodes *S* (source) and T (terminus or target) to calculate the probability of establishing a path between *S* and *T* by assuming a certain probability *p* (probability of an edge being operational). In ATR mode, the main problem leads to finding the probability of the path between any two desired nodes *u* and *v* of the network. Finally, in the case of KTR, the problem is that if there is a set of *K* distinct nodes with the available number $|K| = k$, what will be the probability of establishing a path between any two nodes.

In this study, according to the nature of the components in the arithmetic circuit, the reliability of the network is practically in the KTR class. However, the cases raised here can be easily extended to other classes and do not create any restrictions. All these three categories are considered to be NP-complete; that is the problems can be solved by a non-deterministic counting Turing machine in polynomial time and are also considered NP-hard. Throughout this research and all the presented methods, our main goal is to calculate the reliability of *K* input and output from network terminals, i.e., KTR, which is defined as follows. In this way, the main problem is reduced to calculating the connectedness probability between a subset of *k* of a graph assuming healthy nodes and the probability of failure in the function of its edges. Reliability of the graph *G* is a function of the vector $P = (p_1, \ldots, p_n)$ that p_i expresses the probability of failure of the edges. This function is denoted by the symbol *h*(*G*, *P*) or *h*(*P*) in short. In this research, we assume that the probability *p* remains constant throughout time and for all edges of the network $e \in E$. However, the probability of failure of each edge such as *f* from another edge such as *e* is independent of each other for all edges of the network $f, e \in E, f \neq e$. We also assume that after failure in the function of each edge, no re-connection will be established between the nodes corresponding to the faulty edge (lack of repairability). For simplicity, it is assumed that the capacity of all network communication links is infinite, which means the information flows passing through the links are negligible compared to the capacity of the entire network. The logical reason for this subject is the difference in the possibility of cascading failures in networks, which may make our analysis of reliability uncontrollable. Certainly, this issue itself is a necessary matter for research, which can be pursued as one of the future works.

3.1 Reliability Polynomial

In this section, after presenting a series of preliminary definitions, reliability polynomials and the calculation method of its coefficients will be presented.

Definition 1 [28]: *Pathset is a subset of edges* $O \subseteq E$ *that causes the graph be integrated; in other words, (V,O) is operational.*

If our problem is of the KTR type, the pathset will contain a connected spanning subgraph consisting of *K* components of the graph *G*. According to the inclusion principle, a set of minimal paths is called minpath. In the case of 2TR, the minimal paths include only a single path between two nodes *S* and *T*, and for the KTR class, it includes a Steiner tree between *K* components, and for ATR, the minimal path will be a spanning tree.

Definition 2 [27, 28]: *The set of all indices of the state vector X in which* $x_i=0$ *is called the cutset. In fact, the cutset is a subset* $C \subseteq E$ *of edges such that the subgraph (V, E\C) is not connected. The minimal cutset vector is also the vector for which the graph will be disconnected.*

Definition 3 [27, 28]: *Let m be the number of edges (size) of the graph G(V,E). For* $E' \subseteq E$*, the reliability polynomial is defined as follows*

$$h(G, p) = \sum_{\substack{E' \subseteq E \\ G' \text{ is a pathset}}} p^{|E'|}(1-p)^{m-|E'|} \tag{1}$$

Thus, *h*(*G*, *p*) represents the probability that the graph *G* is operational in terms of a function of *p*. We note that the reliability polynomial definition is the same in all three modes, 2TR, KTR, and ATR. The only difference in it is related to how to determine the pathset and the cutset. It is also necessary to mention that there are different forms for the reliability polynomial definition, which we will discuss in the following.

Definition 4 (N-form) [27, 29]: *Let* N_i *refer to the number of sets of paths including i edges. In this case, the probability of providing a set of i edges that causes the network to be connected is given by*

$$h(G,p)=\sum_{i=0}^{m} N_i p^i (1-p)^{m-i} \tag{2}$$

Definition 5 (C-form) [27, 29]: *If we assume C_i as the number of cutsets with i edges, then we have*

$$h(G,p)=1-\sum_{i=0}^{m} C_i p^{m-i}(1-p)^i \quad ,N_i+C_i=\binom{m}{i} \tag{3}$$

Definition 6 (F-form) [27, 29]: *An F-set is a set of edges whose complementary set is the pathset. With the help of F-sets, another method can be provided to define the reliability polynomials. The reliability polynomial based on F-set is defined as*

$$h(G,p)=\sum_{i=0}^{m-n+1} F_i p^{m-i}(1-p)^i \quad ,F_i=N_{m-i} \tag{4}$$

where F_i is the number of subsets (subgraphs) that have exactly *i* edges and remain in the network after removing *m-i* edges, and if they are removed, the graph *G* will be disconnected.

Reliability polynomials can be used to compare the reliability of different networks. Certainly, it must be noted that the reliability polynomial does not represent a total ordering in the set of graphs and only defines a partial order. Although the reliability polynomial metric may seem simple in the first step, there are many problems in its calculation. Unlike other robustness measures that attribute a numerical value (usually normalized) to the robustness of the network, the reliability polynomial attributes a function in terms of *p* to the network. One of the major and important challenges is determining the coefficients of reliability polynomial for graphs with large size and order. As well as assigning the correct values to the probability *p* is also important, which is analyzed in more details.

So far, various methods have been proposed to calculate the coefficients of reliability polynomial, some of which were reviewed in Section 2. The main concern of all these algorithms is rooted in their recursion behavior, which increases the computational complexity. Hence, if the number of edges (or more precisely, the difference between the number of edges and nodes of the graph) exceeds a certain amount, the exact calculation of coefficients practically becomes an NP-hard problem. It can be concluded that almost none of the algorithms for determining coefficients can be practical for a complex network, especially with relatively large dimensions. However, since the size and order of the logical circuits that we are dealing with in this study are not very large, the algorithms presented in [27], which are based on random algorithms and interpolation, are suitable enough for our purpose in this research. However, to estimate the reliability of arithmetic circuits with larger order and size, we will face practically the same basic concerns.

4. Hammock-based Networks

In this section, with studying the reliability polynomials of minimal Hammock networks, we will investigate the reliability polynomial of basic logical gates. We mentioned that the main goal of Moore and Shannon [6] was to improve the reliability of the network by replacing a single unreliable two-contact electromechanical relay (switching element) with an extended network of similar relays. The relay can be in the normal-open (NO) or normal-close (NC) state. Usually, if the pair of contacts is not in contact with each other, it is known as NO state; otherwise, if they are in contact with each other, it is known as NC. In fact, the NO and NC states are the state of the electrical contacts when the coil is de-energized; in other words, the voltage source is not connected to the coil. In this way, relays can be considered as elements of binary electrical switches; however, today there is not this type of relays in circuits and they have been replaced by the conventional electronic switching elements, i.e., *n* and *p* type of CMOS transistors.

Let *a* represent the probability that the coil is energized and the contacts are closed, and *c* denotes the probability that the coil is not energized so the contacts are closed. Figure 1 illustrates this from the perspective of a binary channel. To reproduce the study of Moore and Shannon, the coil is simulated with a pMOS transistor. The energization of the coil is assumed to be equivalent to placing "1" in the pMOS gate, and when the coil is not energized, it will be considered equivalent to placing "0" in the pMOS gate.

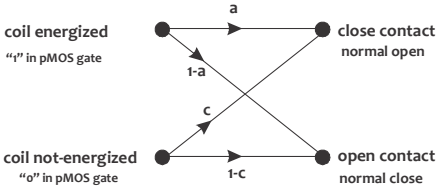

Figure 1: Schematic representation of transition possibilities in the relay (switching element) [6]

In Figure 1, the transition rate occurs with the probability of a ($a>c$) and the breaking contact or normal-close (the coil is de-energized) is also equivalent to setting zero in the pMOS gate and establishing current between the two contacts, which occurs with probability $c>a$. This means that with a probability greater than c, a short path will be established between S and T. In this way, any network consisting of MOS transistors can be assumed to be a binary channel. It is assumed that all coils throughout the circuit are simultaneously (synchronously) energized/de-energized. For the binary channel shown in Figure 1, the channel transfer matrix can be written as

$$Q=\begin{pmatrix}1-a & a\\ 1-c & c\end{pmatrix};a,c\in[0,1] \tag{5}$$

The goal of Moore and Shannon of such an arrangement and assumptions was to investigate the possibility of a path or establishing a connection between input and output. In a network with n relays (type of transistor: p or n), if the coil is not energized ("0" in the pMOS gate), the path is established with a probability greater than c; if the coil is energized ("1" in pMOS gate), the path will be established between S and T with probability less than a (see Figure 1). Moore and Shannon called these relays as crummy; what they meant by this naming was that if $a=c$, this is equivalent to a binary noisy channel in which the amount of ambiguity has reached its maximum and as a result the channel capacity will be zero ($C(a,c)=0$).

If we draw the reliability curve of the networks, we will see that all the networks tend to improve in reliability to zero or 1 values around the point p. In Figure 2, it is clear that the reliability diagram intersects the diagonal line at the point p between the two assumed values a and c. However, it does not matter how close these two points are to each other. As can be seen, the reliability function for point a is smaller than the positive constant value δ and for point c it is greater than $1-\delta$. This means that any suitable network can be made of a sufficient number of crummy relays.

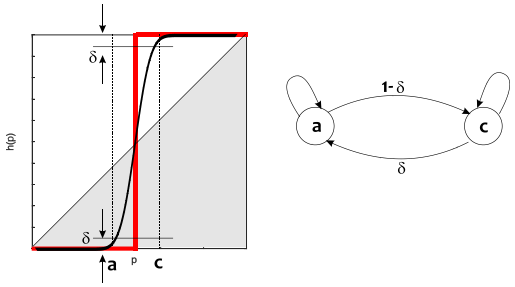

Figure 2: Reliability function and the corresponding state transition diagram [6]

Therefore, Moore and Shannon assumed that $a\neq c$. That means if the relays are supposed to be closed, the reliability (probability) of their closing is high, and similarly, if they are supposed to be open, they are more reliably (probably) open ($a\to 0$ and $c\to 1$ and $a<c$). Accordingly, in short, Moore and Shannon have conditionally stated the two possibilities to ensure the correct operation of the device (relay element).

$$\begin{aligned}&\mathrm{P}\{\text{normal-open/coil energized}\}=a\\&\mathrm{P}\{\text{normal-open/coil not-energized}\}=c\end{aligned} \tag{6}$$

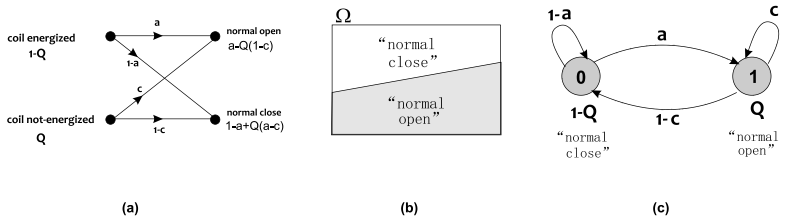

Figure 3: (a) illustration of a binary channel corresponding to a switching element (relay/transistor); Q is the probability of the coil being in an energized state and $1-Q$ is the probability of its complement; (b) the Bayesian probability space corresponding to the normal-open (NO) and normal-close (NC) states; (c) state transition diagram corresponding to the binary channel depicted in (a)

The probabilities a and c in Equation (6) are defined as conditional probabilities for a two-terminal switching element (relay/transistor) and divide the Bayesian probability space into two nonempty and disjoint subsets; i.e., "normal-close" and "normal-open". The applied network will contain a sequence of independent and identical (i.i.d) random variables whose probability of being "closed" is equal to p and the probability of being "open" is assumed to be equal to $q=1-p$. Each network will be like a Boolean function composed of Bernoulli random variables. Since it is symmetrical, it will not be affected our interpretation of the probability of p or q. The main question of Moore and Shannon was what is the reliability function of a

network consisting of *n* number of these components and how can the total reliability of such a network be calculated using the total Bayesian space consisting of binary independent random variables.

In Section 2, we mentioned that the reliability polynomial function, denoted by $h(p, G)$ or $h(p)$ in short, is a function of degree *n* (the number of relays/transistors in the circuit or edges in graph *G*), which shows the probability of being "closed" or having a path in the network between two points of origin *S* and terminus *T*. Thus, in the general case, we face with successive trials of the Bernoulli distribution, which leads the reliability polynomial to the binomial distribution. So, the shape of the reliability curve $h(p)$ is similar to the binomial distribution function.

Moore and Shannon proved that the reliability polynomial curve $y=h(p)$ can intersect the line $y=p$ (simple system reliability) at a certain point like $p_0 \in (0,1)$. It is necessary to mention that in the ideal case, the reliability curve $h(p)$ is a unit step function that is located between 0 and 1 and passes through the point p_0. The closer the function $h(p)$ extracted from the circuit is to this ideal step function, the more accurate and clear the reliability calculations will be. In practice, $h(p)$ is a polynomial function in terms of *p* and it can only be approximated by the step function. Usually, larger and more complex networks and circuits can be obtained by connecting smaller Hammock networks in series, parallel, and combination. Moore and Shannon presented that such combinations in networks can improve the reliability function $h(p)$. With a sufficiently large number of iterations, the ideal step function can be reached. In systems where the reliability curve $h(p)$ intersects the diagonal line once, the improvement in reliability can be displayed with better clarity with the method of combination or staircase construction (the von Neumann approach).

Each Hammock network consists of *w* parallel rows consisting of *l* series relays; there are *l* columns and *w* rows with matchstick placed between them (see Figure 4). Usually, the cost of building and implementing Hammock networks is expressed by the number of relays (transistors) used in it; i.e., $l \times w$, and this issue leads us to the definition and use of minimal Hammock networks (lower cost). It has been shown that [7] there is $(B_w)^{l-1}$ minimal Hammock network with width *w* and length *l*, where B_w represents the w^{th} Bell number, which refers to the number of elements in a set with *w* members.

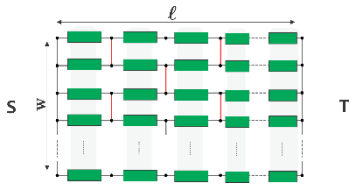

Figure 4: Schematic representation of the Hammock network, $H_{w,l}$, the input and output terminals are marked with *S* and *T*, respectively, and the vertical lines are called matchstick.

As shown in Figure 4, between the parallel lines, a series of fine vertical wires are placed for connection, which are called matchsticks. The number of these matchsticks is equal to $(w-1)(l-1)$. Throughout this paper, it is assumed that these matchsticks do not suffer from the failure can only occur with the probability of *p* in the operation of relays (transistors). In this way, there is $2^{(w-1)(l-1)}$ Hammock networks, which is clearly much smaller than $(B_w)^{l-1}$, the minimum number of Hammock networks.

For distribution of matchsticks, two limits can be considered. The lower bound is the full mesh network, in which there is no any matchstick. The upper bound is an arrangement in which all possible states exist for having $(w-1)(l-1)$ matchsticks. Assuming that the distribution of match sticks in Hammock networks is uniform, $(w-1)(l-1)$ matchsticks are in half of the arrangements and absent in the other half, by average. Thus, there will be $(w-1)(l-1)/2$ matchsticks. In order for the number of these matchsticks to always be an integer, it is possible to consider a design like a brick-wall for Hammock networks in two cases. Hence, a small distinction is made for the two arrangements. The following definitions refer to these two arrangements.

Definition 7 [7]**:** *Hammock network with width w and length l is displayed with the symbol* $H_{w,l}$*, whenever the value* $\lfloor (w-1)(l-1)/2 \rfloor$ *is an integer.*

Definition 8 [7]**:** *Hammock network with width w and length l is denoted by* $H^{+}_{w,l}$ *if the value* $\lceil (w-1)(l-1)/2 \rceil$ *is an integer.*

For example, the Hammock network shown in Figure 5 (a) has 3 matchsticks, denoted by the symbol $H_{4,4}$ according to Definition 7; while the arrangement of matchsticks in Figure 5 (b) includes 4 matchsticks, which is expressed by symbol $H^{+}_{4,4}$ according to Definition 8.

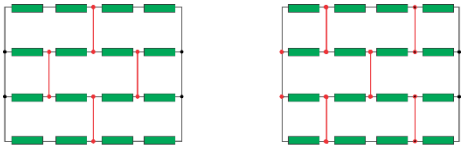

Figure 5: Two layouts of 4×4 Hammocks; (a) Hammock network $H_{4,4}$; (b) Hammock network $H^{+}_{4,4}$

At the end of this section, it is noteworthy to mention that we have only done polynomial estimation of the reliability of circuits based on minimal Hammock networks. Thus, the other issues related to the design aspects such as process variation, aging as well as temperature have not been included as the index factors in the reliability analysis. These are among the important factors that deserve to be evaluated in a separate research along with other reliability evaluation measures.

4.1 Reliability Polynomial of Hammock-based Networks

In Section 3.1, we mentioned that several forms have been suggested to calculate the reliability function $h(p)$ in a network. In this section, we will examine these cases again focusing on the calculation of reliability polynomial coefficients for Hammock networks with width w and length l. Among the proposed forms, the following two forms can be more useful for our goal; however, the use of other forms also leads us to similar results.

$$\begin{cases} h(p) = \sum_{k=l}^{n=wl} P_k . p^k \\ h(p) = f(p,q) = \sum_{k=l}^{n=wl} N_k p^k q^{n-k} \end{cases} \tag{7}$$

The first form in Equation (7), which is called P-form for short; it is written based on the generating function where q=1–p and N_k represents the number of ways in which a subset of k contacts (transistors) can be selected in the network in such a way that if k contacts are closed and the rest n–k contacts are open, the entire network remains "closed". In other words, N_k is the number of subsets of k relays (transistors) that will establish a path from S to T. The above equation, obviously, means the summation over the probability of all the distinct ways under which the network remains "closed." From Equation (7), for the first and second coefficients, it can be written as

$$\begin{cases} P_l = N_l \\ P_{l+1} = -(wl - l)N_l + N_{l+1} \end{cases} \tag{8}$$

Equation (8) shows the relationship between the first and the second coefficients, that is, P_l and P_{l+1}, in N and P forms. In fact, N_l is the number of paths in the brick-wall-network, in a rectangle with width w and length l (Hammock network $H_{w,l}$) and the term P_{l+1} represents the number of subsets of l+1 members of relays (transistors) that are counted by N_{l+1}. w_{l-1}, the remaining possible relays (transistor) are counted by N_l ways and therefore multiplied by N_l. It is important to mention that there is another form known as C-form, which is given by [7]

$$\begin{cases} h(q) = \sum_{k=w}^{n=wl} H_k . q^k \\ h(p) = g(p,q) = 1 - \sum_{k=w}^{n=wl} C_k q^k p^{n-k} \end{cases} \tag{9}$$

The following relationship exists between N-form and C-form.

$$N_k + C_{n-k} = \binom{n}{k} = \frac{n!}{k!(n-k)!} \tag{10}$$

Moore and Shannon [6] have introduced 29 minimal Hammock networks, which their diagram and the reliability polynomial coefficients have been calculated in [7] as well. We note that the coefficient of the term corresponding to the lower power in the polynomial refers to the number of Steiner trees corresponding to the Hammock network.

Hammock networks are rectangular networks with width w and length l. Therefore, Equations (7) to (10) from an intuitive point of view mean that the more the number of parallel components in the network, the more reliability in the "closed-circuit" mode. Conversely, the more series components in the network, the more reliable network will be in "open-circuit" mode. Obviously, according to the simulation results, we will see that the quality of parallelism in Hammock networks is directly related to the width w; since this quantity represents the minimum number of relays (transistors) that must be open so that the network remains in "normal-open" mode. In other words, the parameter w refers to the size of the "minimum cut" separating the source S from the terminus T. Similarly, the quality of the serial networks is related to the parameter l which represents the minimum

number of relays (transistors) that are required to be "closed" so that the entire network remains in the "normal-closed" state. For simplicity, l denotes the size of the "pathset" between S and T. Larger values of l cause the more $p \to 0$, the more $h(p)$ values decrease towards zero. Similarly, the more w increases, with $p \to 1$, the reliability polynomial values of $h(p)$ tend towards 1 faster. In general, in the case of Hammock networks, we can conclude that the larger values of l and w, the curve of the reliability function of the network will be closer to the ideal step function (optimal network).

4.2 Reliability Evaluation of Hammock-based Networks

Fault-tolerance is a key issue for evaluating any network. Due to the failure, nodes and edges may be removed from the network and as a result, local or global characteristics of the network as well as its correct operation may be changed. Faults and failures may not only reduce the operational and computational power of the network, but also may alter the topology of it and lead to disintegration.

In this section, we are going to introduce some of the most important criteria and present how the reliability of networks can be evaluated and compared with each other by measuring and interpreting them. The effort is to provide a precise, appropriate and consistent classification of the criteria, while expressing the advantages and disadvantages of each, we can benefit from the interpretation of the criteria in an efficient manner.

In selection and classification of reliability measures, a wide range of keywords related to reliability and dependability has been searched in the related work. There are many metrics, some of which share similar characteristics, while a natural question is how can the measure be divided into appropriate categories without overlapping? Briefly, in the selection of reliability criteria, three issues are mainly considered

(i) The ability to apply the desired criterion on the type of graph
(ii) Direct measurement of known aspects of graph reliability
(iii) The existence of a clear and specific relationship between the chosen reliability criterion and the characteristics of the underlying network

In this way, the desired characteristics in the selection and extraction of measures can be summarized in five categories

1) Graph type (simple, weighted/unweighted, directed/undirected)
2) Global or locality of the criterion (focusing on the connectivity of individual nodes or extracting features about the entire graph)
3) Static or dynamic being the evaluated network
4) The co-domain of the reliability criterion
5) The computability of the reliability criterion (NP-hard or NP-complete).

Thus, in the classification of reliability criteria used in this research, the criteria are mainly in the category of distance based criteria and criteria based on minimum cut. In the following, we will introduce reliability measures to evaluate the reliability of Hammock networks.

One of the simplest and most straightforward measure is to draw the reliability curve $h(p)$ in terms of p, which gives a S-like shape that can be used to compare the reliability of different circuits. The bisector line of the first quadrant also indicates the reliability of a simple system, i.e., $y=h(p)=p$, which represents a single crummy relay (single transistor). Drawing other reliability curves corresponding to the networks and comparing them with the bisector line of the first quarter will demonstrate how much the reliability of the Hammock networks consisting of these relays (transistors) in comparison with the single relay system has been improved. In addition, the performance measure related to measure the reliability of Hammock networks can be divided into three main categories

(i) Performance measures related to reliability improvement such as RII[5], FoM[6], variance and average of reliability
(ii) Performance measures related to improvement in steepness of reliability such as $h'(p)$
(iii) Performance measures related to improvement in the information capacity of the circuit such as CII[7].

In what follows, we will describe these metrics with their calculation and evaluation method.

4.2.1 Improving the Reliability Metrics of Networks

One of the effective measures used to evaluate the reliability of basic logical gates is a measure called RII, which was introduced and used by Klaschka [30]. This criterion is defined as

[5] Reliability Improvement Index
[6] Figure of Merit
[7] Capacity Improvement Index

$$\mathrm{RII} = \frac{\log(p)}{\log[h(p)]} \tag{11}$$

In the next section, the construction method of the logical gates based on minimal Hammock networks will be described. The cost of redundancy in such circuits is expressed by the factor $w \times l$, which is the product of the width and the length of the minimal Hammock network. The next goal of reliability evaluation can be to find an optimal redundancy plan corresponding to the maximum RII criterion under a certain cost, i.e., minimizing the cost for a given RII. Therefore, another metric related to the reliability improvement is defined as FoM, which is the ratio of reliability improvement to the cost of circuit which is defined as [7]

$$\mathrm{FoM} = \frac{\mathrm{RII}}{\mathrm{cost}} \tag{12}$$

For each gate or circuit based on minimal Hammock networks, both reliability measures, namely RII and FoM, can be determined.

Another metric that is similar to FoM is the variance of reliability in a certain interval. This indicator can be defined as

$$\mathrm{varh}(p) = h(1-p_0) - h(p_0) \tag{13}$$

Generally, this metric is considered symmetrically around the point p_0=0.5 (ideal step function). In this way, the above equation can be rewritten as

$$\mathrm{varh}(\varepsilon) = h(0.5+\varepsilon) - h(0.5-\varepsilon) \tag{14}$$

It can be seen that; the value of the variance depends on the parameter ε and is equal to the difference in the area under the curve h between $0.5-\varepsilon$ and $0.5+\varepsilon$. In this paper, we have assumed the parameter ε=0.25, which actually gives the difference between $h(0.75)$ and $h(0.25)$; viz., the third and the first quartiles of the reliability function.

In reliability applications, when there is no knowledge about the probability value p, how can we make a correct decision about the reliability of the network? Brown et al. [31] have introduced and investigated a measure called average reliability polynomial, that is, integral of the reliability polynomial over the interval [0,1]. Their proposed measure is actually an option for uniformly reliable networks. However, the calculation of the average reliability as shown in [31] belongs to the class of NP-hard problems and is a difficult issue in itself; the authors have presented some strategies for bounding the average reliability, which necessarily do not require accurate calculation of reliability polynomial coefficients.

The average reliability of the network is denoted by $avgh(p)$. This measure calculates the average value of the network reliability between both the source and destination terminals in the interval [0, 1]. In fact, calculating the average reliability value for each graph is not practical in general; however, it is possible to calculate the average reliability for Hammock networks such as logical gates and multipliers, and it has been proven that this measure is bounded. That means it can be used as an efficient index in evaluating the reliability of the circuits.

Definition 9 [31]: *The average reliability of graph G expressed by the symbol avgh(p) is defined as*

$$\mathrm{avg}h(p) = \int_0^1 h(p)dp \tag{15}$$

For example, it has been shown that the average reliability of a tree of order n is equal to $1/n$, and for the cycle of order n, C_n, is equal to $2/(n+1)$. It is shown in [31] that if we have two networks G_1 and G_2 such that $h_{G_1}(p) \geq h_{G_2}(p)$ for $p \in [0, 1]$, then $\mathrm{avg}h_{G_1}(p) \geq \mathrm{avg}h_{G_2}(p)$. This shows that this criterion can be as an effective measure to compare the reliability of two networks. When it is not possible to compare networks from the point of view of reliability with the help of the $h(p)$, the average reliability measure can work very effectively and give consistent results. Moreover, like the definition of speed-dup, it can be a measure for the relative comparison of two networks [31].

4.2.2 Improving the Steepness of Network Reliability

The aim of Moore and Shannon is to replace a single relay with a network of relays. Their ideal function was a step function. In this way, the velocity and slope of the curve of reliability or derivative of it, $h'(p)$, can be very important measure in evaluating the reliability of circuits. The derivative of the reliability function shows the steepness and response time of the circuits to the input of the unit step function. Its physical interpretation is the velocity quantity, which we know is expressed by the derivative of the distance. However, for calculating the reliability polynomial inflection points, the second derivative, $h''(p)$, can be used, which means the acceleration in the slope and direction of the curve. On the other hand, if we draw the derivative function of the reliability polynomial, the maximum of it can be dependent with the cost function. Since, at the maximum point of the derivative of reliability, the variation of the ideal step function will be infinite.

In short, the performance measures of the first category mostly deal with the optimal networks in which parallelism is more prominent. However, as the derivative of reliability has increased and is less skewed compared to the normal curve; we will achieve more symmetrical and optimal networks, i.e., balanced and equal l and w.

4.2.3 Improving the Effective Channel Capacity of Networks

Another performance measure of the network reliability which consists of unreliable components such as relays (transistors) is the effective channel capacity denoted by *C*. As stated by Shannon and Moore, the common mode of the coils can be considered as the input of the channel and the connection (establishing a path between *S* and *T*) as the output of the channel. Shannon and Moore, with the exception of some special cases such as the symmetric binary channel with a probability of $c=1-a$ as well as a noisy channel ($a=c$ and as a result C (a, c) =0), have not provided an explicit equation to calculate the channel capacity according to probabilities *a* and *c*. However, Muruga [32] and Silverman [33] have estimated the channel capacity for some binary channels. According to Shannon's definition, the average information on the input symbol of a discrete and memoryless channel that transmits symbols at a specified symbol rate per second is related to the random variable entropy of the channel output. According to the binary channel transmission matrix shown in Figure 3 (a), the transmission rate *R* (bits/symbol) can be calculated from the difference in entropy output of the discrete memoryless channel. In mathematical terms, we get

$$R = H(y) - H(s) = -[a - Q(1-c)]\log_2[a - Q(1-c)] + [1 - a + Q(a-c)]\log_2[1 - a + Q(a-c)] \qquad (16)$$

The main goal is to maximize the rate of information transfer through the channel. According to Shannon's definition, the effective capacity of the channel is the maximum rate of information transmission, and thus it is necessary to maximize Equation (16). By considering the appropriate values and assigning them to the parameters *a*, *c*, *Q*, the maximum effective capacity of the channel can be calculated for a single switching element of the Hammock network, i.e., $H_{1,1}$. In [7] and [34], the authors presented an equation based on the parameters of which the channel capacity can be calculated in terms of bit units in the symbol transmitted from the network. In this way, the capacity of the binary channel can be presented for the relay (transistor) in terms of the possibilities of *a* and *c* where $a, c \in [0, 1]$.

If the binary channel is reliable and perfect, then its capacity will be equal to 1 bit per symbol. However, for an unreliable channel, the effective capacity is a number between 0 and 1. Also, for any network that consists of a number of switching components (single relay or transistor), if its reliability polynomial is $h(p)$, the network capacity is equal to C($h(a)$, $h(c)$). For the simple Hammock network without redundancy, i.e., $H_{1,1}$, its capacity can be calculated in terms of *a* and *c*. The measure of improved reliability performance that is related to the channel capacity is called CII, which can be defined from the following equation [7].

$$\mathrm{CII} = \frac{C(H_{w,l})}{C(H_{1,1})} = \frac{C(h(a), h(c))}{C(a,c)} \qquad (17)$$

The above indicator is a normalized measure. This means that the effective capacity of the network is normalized to the capacity of the simple Hammock network without redundancy (i.e., $H_{1,1}$).

5. Design and Implementation of Minimal Hammock-based Logical Gates

In Section 2, the concepts of reliability and the methods of determining the coefficients of reliability polynomial were presented. Moreover, in this section, the minimal Hammock networks were introduced in details, and in addition to extracting their properties, the method of determining reliability polynomial coefficients has been presented. Further, in Section 4, performance measures were presented to evaluate the reliability of circuits whose design and implementation is based on minimal Hammock networks. The purpose of this section will be to focus more on the theoretical, algorithmic aspects and methods of designing basic logical gates based on minimal Hammock networks. These small networks perform well for array-based architectures. For this reason, we will first design and implement all basic logical gates according to minimal Hammock networks and then evaluate their reliability with the help of reliability polynomials and the metrics introduced in Section 4.2.

The reliability of gates and circuits has been evaluated in terms of the reliability polynomial, which is a function of the probability of correct/incorrect switching of the nMOS and pMOS transistors. This is a new research that has not been done so far at the gate level from the perspective of reliability. In the following, we first utilize minimal Hammock networks to design and implement nMOS and pMOS transistors that are applied in CMOS-based combinational circuits. Then, with the help of minimal Hammock networks and gate transistor design, all basic logical gates and other circuits can be implemented and analyzed for the reliability aspects.

5.1 Transistor Fabrication using Minimal Hammock Networks

In this section, we will present an implementation method based on minimal Hammock networks for the design and fabrication of nMOS and pMOS transistors, which are used in CMOS-based circuits. There are many factors for construction and implementation, which in this research is more emphasized on theoretical and mathematical aspects of calculations.

In order to design and manufacture CMOS transistors, we use their resistance equivalent. For this purpose, an nMOS transistor can be assumed to be equivalent to a simple resistor that its minimal Hammock network is equivalent to $H_{1,1}$. Since the redundancy scheme is utilized to increase the reliability of the circuits, it is possible to consider the equivalent scheme with the redundancies of 2, 3 or 4 parallel resistors. Figure 6 demonstrates the equivalent of resistance network to a single nMOS transistor.

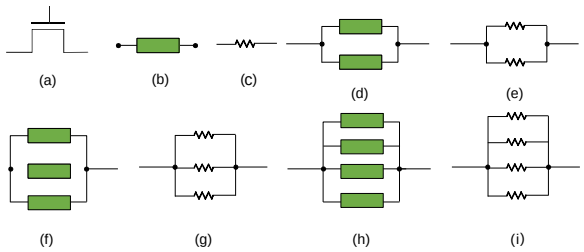

Figure 6: The steps of constructing a single nMOS transistor equivalent to the minimal Hammock network; (a) *n*-type single transistor, (b) minimal Hammock network $H_{1,1}$, (c) equivalent resistance circuit, (d) Hammock network $H_{2,1}$, (e) equivalent resistance circuit with redundancy of 2, (f) Hammock network $H_{3,1}$, (g) equivalent resistance circuit with redundancy of 3, (h) Hammock network $H_{4,1}$, (i) equivalent resistance circuit with redundancy of 4

Similarly, to construct a *p*-type transistor, one can use the same design as the *n*-type transistor. It should only be noted that in order to distinguish between the two types of transistors from the point of view of construction, the approximation of the effective equivalent resistance of the *p*-transistor, which is approximately 3 times that of the *n*-type, has been applied here. In other words, $R_{pMOS} \approx 3R_{nMOS}$. Thus, three different combinations (minimal Hammock networks) with redundancies of 2, 3 or 4 can be considered for the *p*-base transistor. All the possible combinations are illustrated in Figure 7.

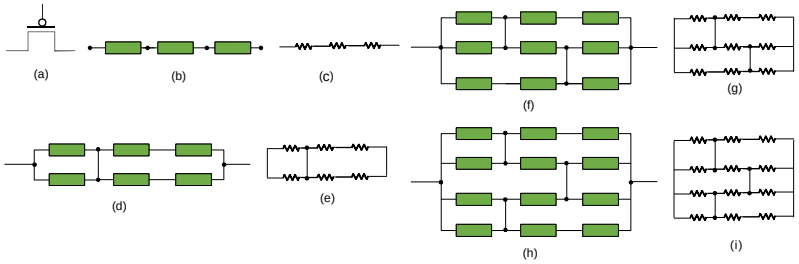

Figure 7: The steps of constructing a single pMOS transistor with the help of the minimal Hammock equivalent network; (a) p-type single transistor, (b) minimal Hammock $H_{1,3}$, (c) equivalent resistance circuit, (d) Hammock network $H^{+}_{2,3}$, (e) equivalent resistance circuit with redundancy of 2, (f) Hammock network $H_{3,3}$, (g) circuit resistance equivalent to redundancy of 3, (h) Hammock network $H^{+}_{4,3}$, (i) resistance circuit equivalent to redundancy of 4

5.2 Fabrication of Basic Logical Gates using Minimal Hammock Networks

After designing and manufacturing the *n* and *p* type transistors with the help of minimal Hammock networks, as described in the previous section, now with the transistor design of the basic gates, one can design and implement all the transistor-based logical gates using the Hammock networks. In this way, we will be able to evaluate and analyze the reliability of the circuits with the help of performance measures, which we have already learned about. In what follows, we will refer to the process of construction the networks and then analyze the reliability of such systems.

Inverter Gate (NOT)

Figure 8 reveals the transistor layout and block diagram of the inverter gate in terms of *n* and *p*-type transistors, as well as the corresponding minimal Hammock network. It should be noted that in order to avoid increasing the cost of all gates and networks, the map of redundancy of 2 has been utilized for both types of *n* and *p* transistors. Obviously, higher reliability can be achieved by using higher redundancies.

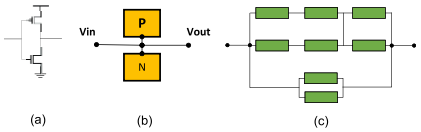

Figure 8: (a) Transistor arrangement of inverter gate; (b) Block diagram of the inverter; (c) Minimal Hammock network of the inverter with redundancy of 2

According to Figure 8, the reliability polynomial of the inverter gate can be written as

$$h(p)= H_{2,1} \parallel H^{+}_{2,3} = 1 - ((1- H_{2,1})\times(1- H^{+}_{2,3})) = 1 - ((1-(2p-p^2))\times(1-(4p^3-2p^4-2p^5+p^6))) = p^8 - 4p^7 + 3p^6 + 6p^5 - 10p^4 + 4p^3 - p^2 + 2p \quad (18)$$

Buffer Gate

Figure 9 shows the arrangement of the transistors and the block diagram of the buffer in terms of *n*-type and *p*-type transistors, and finally the minimal Hammock network equivalent to the buffer.

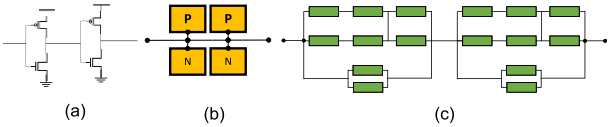

Figure 9: (a) Transistor arrangement of buffer gate; (b) block diagram of the buffer; (c) minimal Hammock network with redundancy of 2

According to Figure 9, the reliability polynomial of the buffer circuit can be calculated as

$$h(p)= (H_{2,1} \parallel H^{+}_{2,3}).(H_{2,1} \parallel H^{+}_{2,3}) = (1 - ((1- H_{2,1})\times(1- H_{2,3}))) \times (1 - ((1- H_{2,1})\times(1- H_{2,3}))) = (1 - ((1- (2p-p^2))\times(1- (4p^3-2p^4-2p^5+p^6)))) \times (1 - ((1- (2p-p^2))\times(1- (4p^3-2p^4-2p^5+p^6)))) = p^{16} - 8p^{15} + 22p^{14} - 12p^{13} - 59p^{12} + 124p^{11} - 58p^{10} - 84p^9 + 126p^8 - 80p^7 + 60p^6 - 48p^5 + 17p^4 - 4p^3 + 4p^2 \quad (19)$$

NAND Gate

Figure 10 (a) shows the block diagram of the NAND gate in terms of *n*-type and *p*-type transistors, and Figure 10 (b) depicts the minimal Hammock network equivalent to the gate.

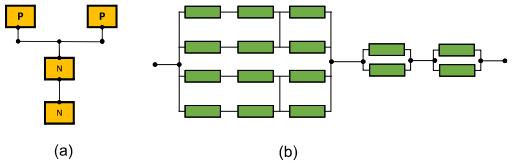

Figure 10: (a) Block diagram of NAND gate; (b) minimal Hammock network of NAND gate with redundancy of 2

According to Figure 10, the reliability polynomial of NAND gate is given by

$$h(p)= (H^{+}_{2,3} \parallel H^{+}_{2,3}).\ H_{2,1}.\ H_{2,1}= (1-((1- H_{2,3})\times(1- H_{2,3})))\times H_{2,1}{}^{+}\times H_{2,1}{}^{+} = (1 - ((1-(4p^3-2p^4-2p^5+p^6))\times(1-(4p^3-2p^4-2p^5+p^6))))\times(2p-p^2)\times(2p-p^2) = -p^{16} + 8p^{15} - 20p^{14} + 76p^{12} - 96p^{11} - 30p^{10} + 116p^9 - 44p^8 + 8p^7 - 48p^6 + 32p^5 \quad (20)$$

NOR Gate

Figures 11 (a) and 11(b) shows the block diagram of the NOR gate in terms of *n*-type and *p*-type transistors, and the equivalent of minimal Hammock network, respectively.

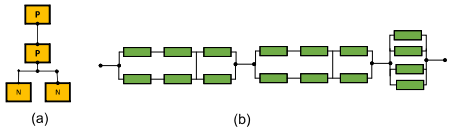

Figure 11: (a) Block diagram of NOR gate; (b) the equivalent of minimal Hammock network with redundancy of 2

According to Figure 11, the NOR gate reliability polynomial can be written as

$$h(p) = H^{+}_{2,3}.\ H^{+}_{2,3}.(H_{2,1} \parallel H_{2,1}) = H_{2,3} \times H_{2,3} \times (1 - ((1 - H_{2,1}^{+}) \times (1 - H_{2,1}^{+}))) = (4p^3 - 2p^4 - 2p^5 + p^6) \times (4p^3 - 2p^4 - 2p^5 + p^6) \times (1 - ((1 - (2p - p^2)) \times (1 - (2p - p^2)))) = -p^{16} + 8p^{15} - 22p^{14} + 12p^{13} + 60p^{12} - 128p^{11} + 56p^{10} + 112p^9 - 160p^8 + 64p^7 \quad (21)$$

XOR Gate

Figure 12 (a) demonstrates the block diagram of the XOR gate in terms of *n*-type and *p*-type transistors, and Figure 12 (b) shows the equivalent minimal Hammock network of the gate.

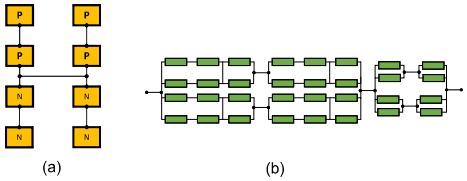

Figure 12: (a) Block diagram of XOR gate; (b) minimal Hammock network of XOR gate with redundancy of 2

According to Figure 12, the XOR gate reliability polynomial can be determined as

$$h(p) = [(H^{+}_{2,3}.\ H^{+}_{2,3}) \parallel (H^{+}_{2,3}.\ H^{+}_{2,3})].[(H_{2,1}.\ H_{2,1}) \parallel (H_{2,1}.\ H_{2,1})] = [(1 - ((1 - (H_{2,3} \times H_{2,3})) \times (1 - (H_{2,3} \times H_{2,3}))))] \times [(1 - ((1 - (H_{2,1}^{+} \times H_{2,1}^{+})) \times (1 - (H_{2,1}^{+} \times H_{2,1}^{+}))))] = [(1 - ((1 - ((4p^3 - 2p^4 - 2p^5 + p^6) \times (4p^3 - 2p^4 - 2p^5 + p^6))) \times (1 - ((4p^3 - 2p^4 - 2p^5 + p^6) \times (4p^3 - 2p^4 - 2p^5 + p^6))))))] \times [(1 - ((1 - ((2p - p^2) \times (2p - p^2))) \times (1 - ((2p - p^2) \times (2p - p^2))))))] = p^{32} - 16p^{31} + 104p^{30} - 320p^{29} + 246p^{28} + 1432p^{27} - 4616p^{26} + 3200p^{25} + 9664p^{24} - 22336p^{23} + 7808p^{22} + 29440p^{21} - 39970p^{20} + 3480p^{19} + 30736p^{18} - 23328p^{17} + 508p^{16} + 5312p^{15} - 656p^{14} - 256p^{13} - 1712p^{12} + 1920p^{11} - 384p^{10} - 512p^9 + 56p^8 \quad (22)$$

OR Gate

Figure 13 (a) shows the block diagram of the OR gate in terms of *n*-type and *p*-type transistors, and Figure 13 (b) shows the minimal Hammock network equivalent to the gate.

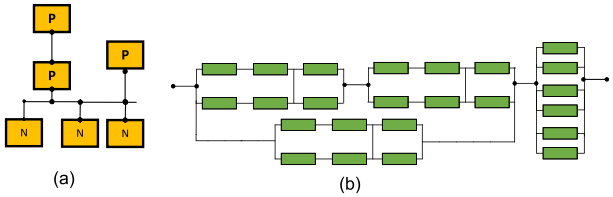

Figure 13: (a) Block diagram of OR gate; (b) minimal Hammock network of OR gate with redundancy of 2

According to Figure 13 and the reliability polynomial of NOT and NOR gates, were calculated in Equations (18) to (21) respectively, the reliability polynomial of the OR gate can be written as

$$h(p) = h_{NOR}(p)\ .\ h_{NOT}(p) = (-p^{16} + 8p^{15} - 22p^{14} + 12p^{13} + 60p^{12} - 128p^{11} + 56p^{10} + 112p^9 - 160p^8 + 64p^7) \times (p^8 - 4p^7 + 3p^6 + 6p^5 - 10p^4 + 4p^3 - p^2 + 2p) = -p^{24} + 12p^{23} - 57p^{22} + 118p^{21} + 4p^{20} - 548p^{19} + 1073p^{18} - 354p^{17} - 1722p^{16} + 2840p^{15} - 1172p^{14} - 1416p^{13} + 2120p^{12} - 1280p^{11} + 640p^{10} - 384p^9 + 128p^8 \quad (23)$$

AND Gate

Figure 14 (a) shows the block diagram of the AND gate in terms of *n*-type and *p*-type transistors, and Figure 14 (b) shows the equivalent minimal Hammock network of the gate.

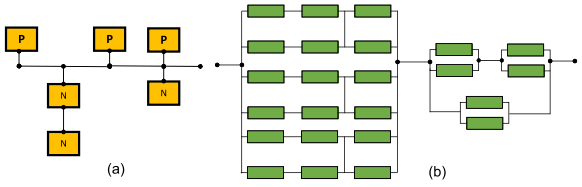

Figure 14: (a) Block diagram of AND gate; (b) minimal Hammock network of AND gate with redundancy of 2

According to the figure and the reliability of NOT and NAND gates which calculated in Equations (18) to (20) respectively, one can determine the AND gate reliability polynomial as

$$h(p)= h_{NAND}(p) \,.\, h_{NOT}(p) = (-p^{16} + 8p^{15} - 20p^{14} + 76p^{12} - 96p^{11} - 30p^{10} + 116p^{9} - 44p^{8} + 8p^{7} - 48p^{6} + 32p^{5}) \times (p^{8} - 4p^{7} + 3p^{6} + 6p^{5} - 10p^{4} + 4p^{3} - p^{2} + 2p) = -p^{24} + 12p^{23} - 55p^{22} + 98p^{21} + 74p^{20} - 604p^{19} + 815p^{18} + 314p^{17} - 1898p^{16} + 1576p^{15} + 324p^{14} - 1048p^{13} + 518p^{12} - 624p^{11} + 980p^{10} - 608p^{9} + 192p^{8} - 128p^{7} + 64p^{6} \quad (24)$$

2:1 Multiplexer

Figure 15 (a) depicts the block diagram of the 2:1 multiplexer in terms of *n*-type and *p*-type transistors, and Figure 15 (b) illustrates the corresponding minimal Hammock network.

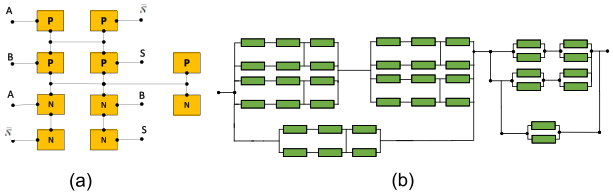

Figure 15: (a) Block diagram of 2:1 MUX; (b) minimal Hammock network of 2:1 MUX with redundancy of 2

According to Figure 15, the reliability polynomial of 2:1 multiplexer can be determined as

$$h(p)= \{[(H^{+}_{2,3} \parallel H^{+}_{2,3}) \,.\, (H^{+}_{2,3} \parallel H^{+}_{2,3})] \parallel H^{+}_{2,3}\}.\{[(H_{2,1} \parallel H_{2,1}) \,.\, (H_{2,1} \parallel H_{2,1})] \parallel H_{2,1}\} =$$

$$= \{[(1-((1- H_{2,3})\times(1- H_{2,3})))\times(1 - ((1- H_{2,3})\times(1- H_{2,3})))] \parallel H_{2,3}\}\times\{[(1 - ((1- H_{2,1}^{+})\times(1- H_{2,1}^{+})))\times(1 - ((1- H_{2,1})\times(1- H_{2,1})))] \parallel H_{2,1}\} =\{(1 - ((1- [(1 - ((1- H_{2,3})\times(1- H_{2,3})))\times(1 - ((1- H_{2,3})\times(1- H_{2,3})))])\times(1- H_{2,3}))))\}\times\{(1 - ((1- [(1 - ((1- H_{2,1}^{+})\times(1- H_{2,1})))\times(1 - ((1- H_{2,1}^{+})\times(1- H_{2,1})))])\times(1- H_{2,1}))))\} = \{(1 - ((1- [(1 - ((1- (4p^3-2p^4-2p^5+p^6))\times(1- (4p^3-2p^4-2p^5+p^6))))\times(1 - ((1- (4p^3-2p^4-2p^5+p^6))\times(1- (4p^3-2p^4-2p^5+p^6)))))])\times(1- (4p^3-2p^4-2p^5+p^6))))\}\times\{(1 - ((1- [(1 - ((1- (2p-p^2))\times(1- (2p-p^2))))\times(1 - ((1- (2p-p^2))\times(1- (2p-p^2)))))])\times(1- (2p-p^2))))\}= -p^{40} + 20p^{39} - 175p^{38} + 850p^{37} - 2278p^{36} + 1852p^{35} + 9145p^{34} - 36050p^{33} + 48410p^{32} + 28644p^{31} - 209558p^{30} + 298840p^{29} - 15708p^{28} - 541712p^{27} + 765747p^{26} - 264958p^{25} - 474544p^{24} + 704096p^{23} - 455588p^{22} + 276248p^{21} - 235012p^{20} + 14992p^{19} + 321616p^{18} - 446016p^{17} + 352513p^{16} - 260556p^{15} + 215163p^{14} - 145826p^{13} + 68446p^{12} - 28460p^{11} + 14788p^{10} - 5304p^{9} - 313p^{8} + 980p^{7} - 354p^{6} + 56p^{5} + 8p^{4} \quad (25)$$

6. Reliability Analysis of Minimal Hammock-based Logical Gates

In this section, using the reliability measures, which introduced in Section 4.2, the reliability of basic logical gates, i.e., inverter, buffer, AND, OR, NAND, NOR, XOR, and 2:1 multiplexer has been evaluated based on minimal Hammock networks.

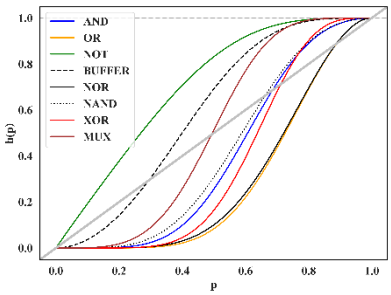

Figure 16: Reliability plots of basic logical gates along with 2:1 multiplexer according to the probability of failure in the switching function of transistors (*p*)

In Figure 16, the reliability polynomial diagrams of the basic logical gates, *h*(*p*), are drawn along with the 2:1 multiplexer. The horizontal axis is in terms of the failure probability of switching elements (relay/transistor) while the vertical axis is in terms of reliability polynomials corresponding to each logical gate, which each of its coefficients have been extracted using Equations (7) to (10). The diagonal line in the figure shows a simple single relay (single transistor) system. As it can be seen, the interesting point is that most of the plots are below the diagonal line for the low values of *p*. This phenomenon reveals that in the area below the diagonal line, there is no a significant improvement in the reliability of the gate compared to the simple system. In other words, there is a small probability that the logical gate based on the minimal Hammock will be closed in comparison with a single relay (transistor). Of course, there are exceptions. As it can be seen, buffer and inverter gates have higher reliability than the other gates. The reason for this issue is the more parallel feature in the networks of these gates. For the sake of clarity, the plots are also drawn in the form of double logarithm on both axes in Figure 17. Again, we see that the highest reliability belongs to the inverting gate; while the OR gate has the lowest rank of reliability and therefore less improvement.

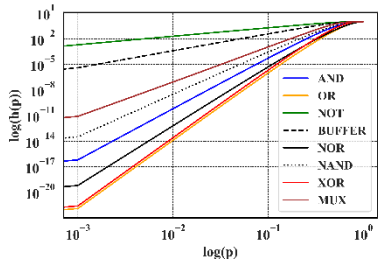

Figure 17: Reliability curves of basic logical gates with 2:1 multiplexer according to the probability of failure in the switching function of transistors (p); both logarithmic axes are drawn.

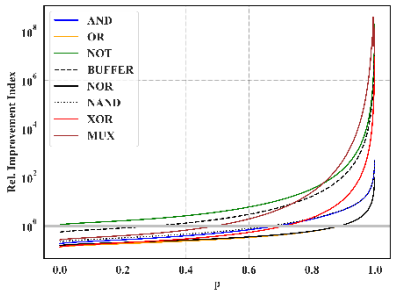

Figure 18: Reliability improvement index (RII) for basic logical gates along with 2:1 multiplexer according to the probability of failure in the switching function of transistors (p); the vertical axis is assumed to be logarithmic.

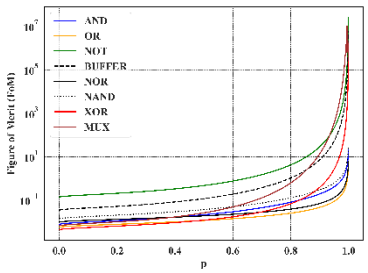

Figure 19: The figure of merit (FoM) index for basic logical gates along with a 2:1 multiplexer according to the probability of failure in the switching performance of transistors (p); the vertical axis is logarithmic.

The parameter RII was introduced in Section 4 by Equation (11). This index is calculated for basic logical gates and displayed in Figure 18. As can be seen in the plots, the least amount of improvement in reliability is devoted to NOR gate and the most of it belongs to multiplexer and inverter gate. It is apparent that, in most of the diagrams, compared to the simple system (y=1), there is an increase in the reliability improvement for p>0.5. FoM was also defined in Equation (12), which is actually normalized to the network cost. According to the definition, the cost of the minimal Hammock network is obtained from the product of its width and its length, which is $w \times l$. In this article, in order to have an estimation of the cost of the circuit, we calculated the total cost from the costs spent on the construction of its components. In this way, the plots in Figure 19 provide us similar information. The lower the cost of wiring in a network, the higher the figure of merit of that network.

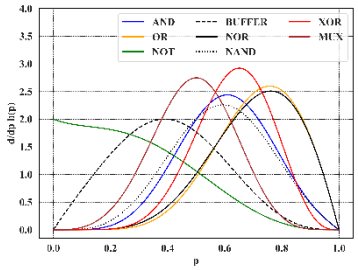

Figure 20: The derivative of the reliability polynomial of basic logical gates along with 2:1 multiplexer according to the probability of failure in the switching function of transistors (p)

In Figure 20, the derivative plots of reliability polynomial are drawn in terms of the probability of failure in the switching function of transistors (p) for basic logical gates along with a 2:1 multiplexer. In Section 4, we mentioned that the derivative of reliability polynomial is a measure that shows the intensity of changes; the higher it is, the closer the network will be to optimality. From the plots in Figure 20, it can clearly see that the XOR gate has the highest reliability derivative. Investigating the structure of the Hammock network of this gate, it can be seen that the XOR gate has an almost square structure; this means that the values of w

and *l* are close to each other and more parallelism can be considered in the structure of this gate. The next circuit in terms of comparison is the 2:1 multiplexer, which has the highest derivative value at a point around 0.5 and shows that it benefits from more parallelism in its structure and the rate of changes at this point depends on the ideal unit step function.

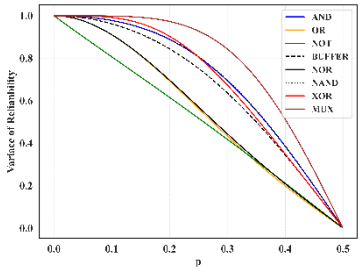

Figure 21: The variance of reliability for basic logical gates along with 2:1 multiplexer in terms of the probability of failure in the switching function of transistors (*p*)

In Figure 21, the variance of reliability polynomial of logical gates and 2:1 multiplexer is drawn in terms of *p* in symmetrical intervals, around the point 0.5 (ideal step function). As we mentioned in Section 4.2, the amount of this variance represents the area under the curve of reliability derivative in a symmetrical interval, which we have calculated for the first and third quartiles of the function. The lower the value of the variance, the closer the reliability of the desired network to the ideal function and the better performance has been presented close to the optimal network.

As we mentioned earlier, another performance index for measuring the reliability of circuits is the effective capacity of the binary network channel. The goal is to maximize the effective capacity of the channel which is the maximum rate of information transmission through the network, and an optimal network is the one for which the amount of information transmission is maximum. The amount of effective capacity of the channel is measured in terms of bit units in the symbol transmitted from the underlying network. The values of capacity are determined and displayed for several logical gates in Figure 22. It is also necessary to mention that for each gate, the corresponding contour diagram is drawn for greater clarity. In summary, what is clear from the plots shown in Figure 22 is that the increase in redundancy of the circuits compared to the inverter gate and single relay (transistor) leads to an increase in improving reliability, speed, and acceleration of information transmission. This fact will lead to a significant improvement in the effective capacity of the network channel.

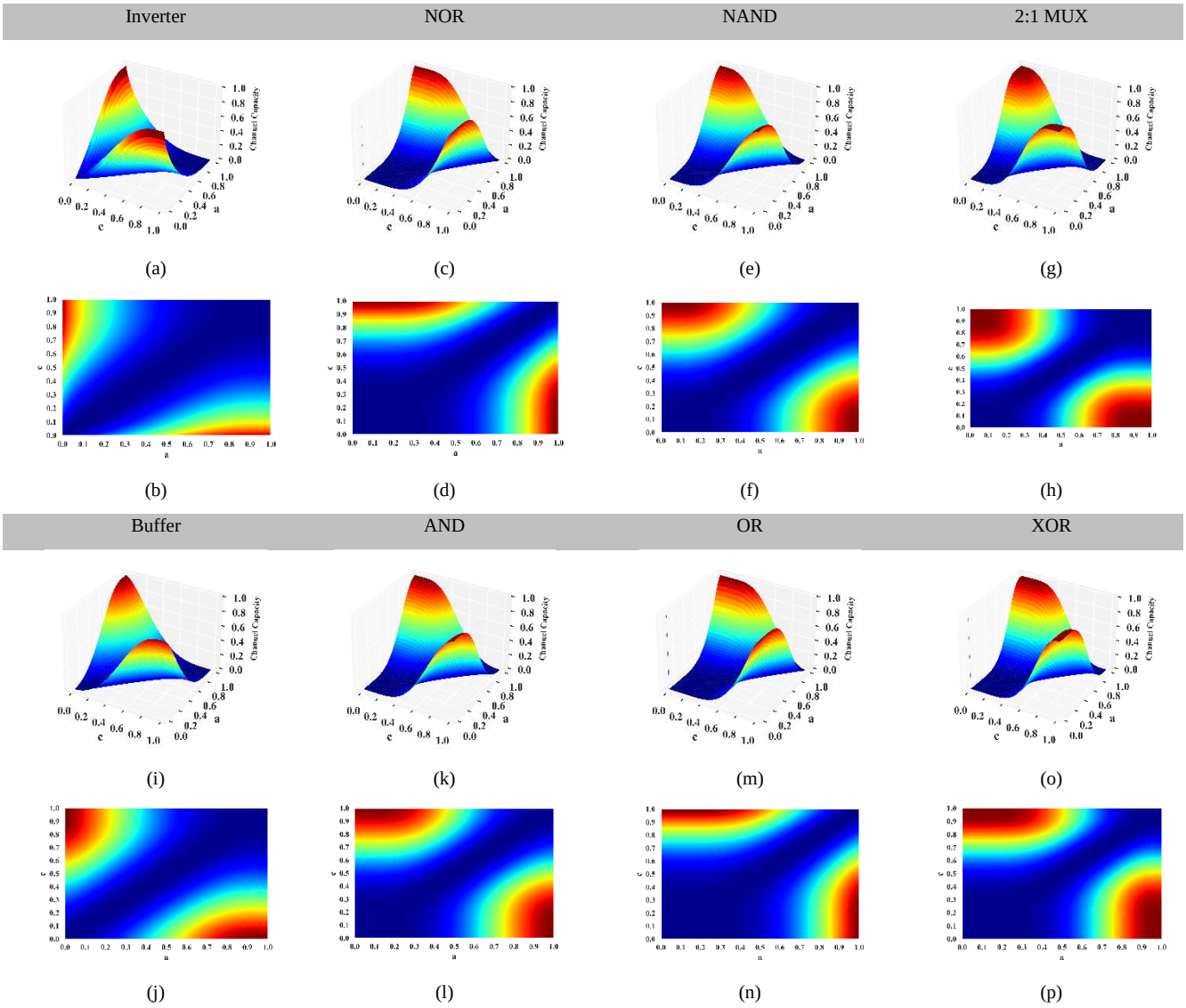

Figure 22: The effective capacity of binary channel for basic logical gates along with 2:1 multiplexer; for each circuit, the corresponding contour diagram is drawn for the sake of greater clarity.

In Figure 23, the diagrams of the channel capacity improvement index, i.e., CII, are drawn for basic logical gates along with a 2:1 multiplexer. The important point in the plots is that the values of effective channel capacity index improvement are normalized to the network channel capacity with no redundancy, i.e., Hammock minimal $H_{1,1}$ for the sake of greater clarity. Additionally, to have a better understanding of the improvement in the effective capacity of the discrete binary channel, for each of the gates, the analogous contour diagrams are also sketched. The contour plots explain the emergence of separation boundaries. The sooner the separation boundaries meet, the greater the increase and improvement in the effective capacity channel have been seen compared to a single transistor. It can be seen from the plots that when both parameters involved in the effective capacity of the gate channel tend to 0 or 1 (i.e., $a,c\rightarrow 0$ or $a,c\rightarrow 1$), there is no any considerable improvement. In other words, increasing the redundancy will not have any effect on improving the effective capacity of the discrete binary channel. For this reason, it can be concluded that in order to increase both the reliability and the effective capacity of the network channel, it is necessary to implement networks only for specific values of a and c parameters.

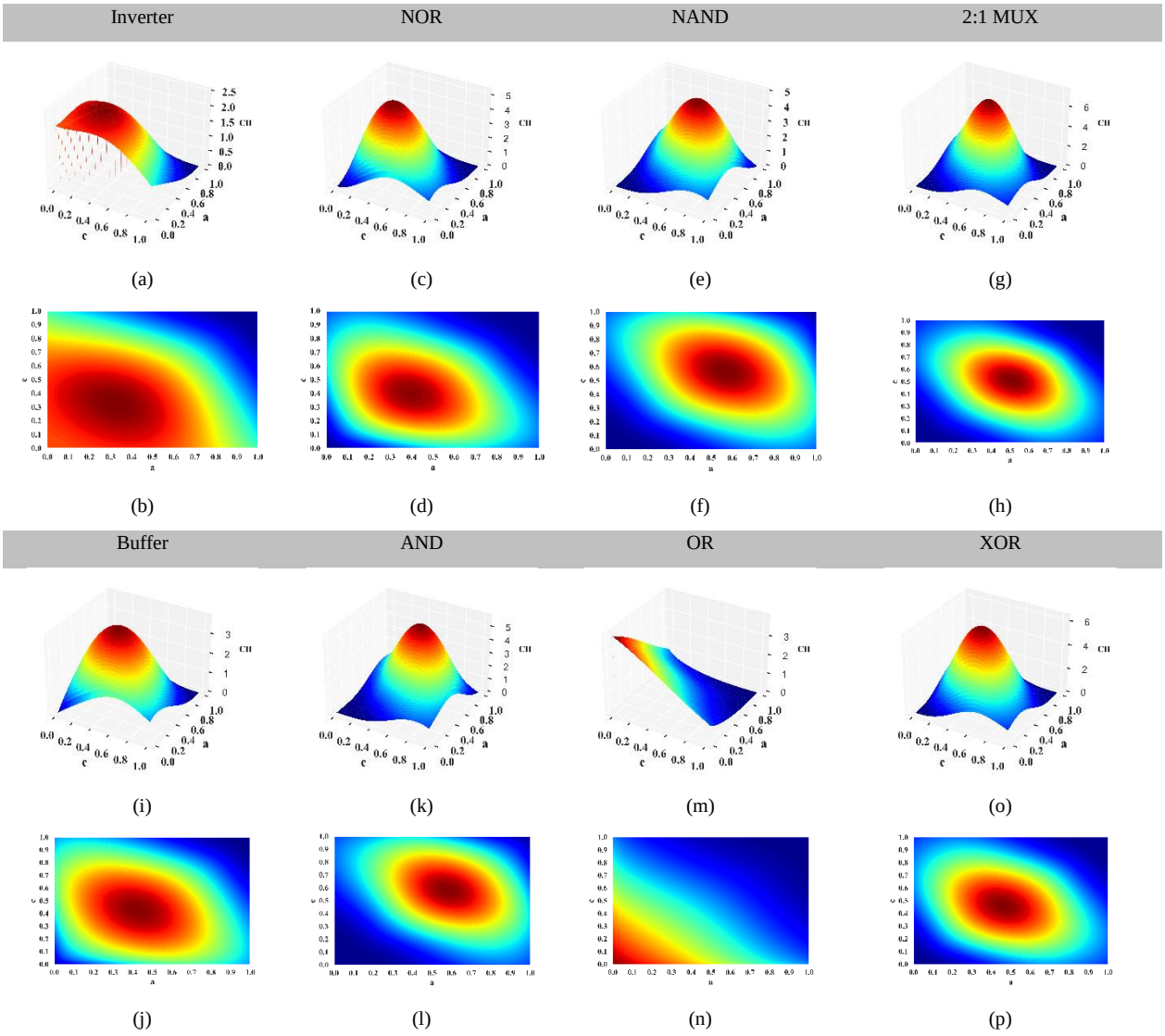

Figure 23: The channel capacity improvement index (CII) for basic logical gates along with 2:1 multiplexer; The values shown are normalized to the non-redundant Hammock channel capacity index, $H_{1,1}$; For each circuit, the corresponding contour diagram is drawn for the sake of greater clarity.

Table 1: Summary of numerical values of performance indicators for basic logical gates based on minimal Hammock networks

		Circuit								
		AND	**OR**	**NOT**	**BUFFER**	**NOR**	**NAND**	**XOR**	**XOR**	**MUX 2:1**
Performance index	**Average reliability**	.3952	.2868	.7063	.5952	.2935	.4140	.3686	.3686	.5075
	Cost	24	24	8	16	16	16	32	32	40
	Reliability variance	.8057	.5628	.5175	.7516	.5704	0.8077	.8051	.8051	.9278

In Table 1, the summary of the numerical values obtained from the simulations of performance measures, i.e., the average reliability, the cost and the variance for all logical gates is calculated. The highest average value of reliability belongs to the inverter gate and the lowest value to the OR gate. Moreover, multiplexer and inverter gates, have the maximum and minimum cost and variance among other logical gates, respectively.

7. Concluding Remarks and Future Research Directions

The reliability of any network is usually expressed based on the tolerance of it against random failures and targeted attacks. Networks are very prone to random failures and systematic attacks; so, evaluating and improving their reliability is considered as one of the important and necessary design aspects. One of the important performance measures is the polynomial reliability. Dislike to the other metrics that assign a numerical value (usually normalized) to a given network, this measure assigns a function

to the graph according to a given probability of edge failure. By determining the coefficients of reliability polynomial, one can access a wide range of facilities and measures for assessing the network reliability. On the other hand, evaluating the reliability of arithmetic circuits based on logical gates has been considered as one of the important research fields in the recent years. Since the performance evaluation of the networks is mainly based on metrics such as speed, area, delay, power-delay product (PDP) and so on, little attention is paid to the analysis of the reliability of such systems which is a very important and necessary consequence. According to the structure of Hammock networks, they can be utilized to design and implementation of array-based designs such as vertical FET (VFET), vertical slit FET (VeSFET), FinFETs, NEMS, as well as array-based structures of CMOS. In this manuscript, we first designed and implemented transistors and basic logical gates with the help of minimal Hammock networks. Then, for all gates, the reliability was extracted with the help of efficient calculation (with low complexity) of reliability polynomial coefficients. It is important to mention that, the proposed approach in this research is not dependent and limited to a special network and it can be used to measure the reliability of other circuits and networks as well.

One of the most important challenges in this research is the efficient calculation of reliability polynomial coefficients. Accurate calculation of such coefficients is efficient only for graphs with low order and size; so, the exact determination of coefficients is included in NP-hard problems. In this way, exploring efficient methods that can reduce the complexity order of algorithms becomes one of the important role and key aspects of the research and the work in this field will continue. Moreover, as other future work that can be done in line with the current research, is that the assumption of independence of failure in network components may seem unrealistic at some cases. For example, in geometric, transportation, and optical telecommunication networks, failures can affect large geographical areas. Failures in such networks are mostly not independent and the joint probability of failures for two or more components with their proximity is correlated. It has also been shown in the networks that the probability of some links will be failed or subjected to a systematic attack depends on the length of the link. That means, in such cases, we will deal with geographically correlated failures. Additionally, several assumptions can usually be done to make network reliability analysis tractable. One of the most common assumptions is that all communication links have the same failure probability distribution. This assumption is obviously unrealistic and as a result, as another future research is to investigate the probability of edge failure with a specific statistical probability distribution can be considered a useful study. Another thing that deserves to be mentioned is that the underlying networks are all of binary type. Each component (node or link) can only be in one of two states: UP (operational) or down (non-operational). However, in practice, we may face situations where other possible situations can be imagined. For example, there are types of networks known as ternary networks, where the state of each component can be in one of three possible states; i.e., UP, down, or middle. Indeed, the third state models the situations that the component works under certain restrictions. Like a link whose bandwidth has been significantly reduced. Decision for a network whether is reliable or not, requires a method to measure the reliability of that network quantitatively. During the past years, various indices have been proposed to measure the degree of networks reliability. However, the researchers in this field have not reached an agreement on which of these criteria is superior to the other. Hence, this need and effort will continue as a valuable field of research. On the other hand, it is possible to focus on the assumptions raised in this analysis to be more compatible with real world scenarios. Also, this method can be extended for sorters and quantum circuits.

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